ABSTRACT OF THE DISCLOSURE

A data processor whose level of operation parallelism is enhanced by composing floating-point inner product execution units to be compatible with SIMD and thereby enhancing the operation processing capability is made possible. An operating system that can significantly enhance the level of operation parallelism per instruction while maintaining the efficiency of the floating-point length-4 vector inner product execution units is to be implemented. The floating-point length-4 vector inner product execution units are defined in the minimum width (32 bits for single precision) even where an extensive operating system becomes available, and compose the inner product execution units to be compatible with SIMD. The mutually augmenting effects of the inner product execution units and SIMD-compatible composition enhances the level of operation parallelism dramatically. Composition of the floating-point length-4 vector inner product execution units to calculate the sum of the inner product of length-4 vectors and scalar to be compatible with SIMD of four in parallel results in a processing capability of 32 FLOPS per cycle.